

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:
  - a scan target block that has at least one scan flip-flop and at least one combinational circuit and that is an object to be scanned;
  - 5 a serial-parallel conversion unit that receives serial scan output data output from the scan flip-flop of the scan target block and converts the serial scan output data into parallel scan output data; and
  - a scan output storage that temporarily stores the parallel scan output data output from the serial-parallel conversion unit and outputs
  - 10 the parallel scan output data at a predetermined timing.
2. The semiconductor integrated circuit according to claim 1, wherein the scan output storage outputs the parallel scan output data to outside of the semiconductor integrated circuit at the predetermined
- 15 timing.
3. The semiconductor integrated circuit according to claim 1, further comprising:
  - a scan input storage that stores parallel scan input data; and
  - 20 a parallel-serial conversion unit that receives the parallel scan input data stored in the scan input storage, converts the parallel scan input data into serial scan input data, and inputs the serial scan input data into the scan flip-flop of the scan target block.

4. The semiconductor integrated circuit according to claim 1,  
further comprising:

an expected value storage that stores an expected value of the  
parallel scan output data; and

5 a comparison unit that receives the parallel scan output data  
from the scan output storage and the expected value from the expected  
value storage, compares the parallel scan output data and expected  
value, and outputs a result of comparison.

10 5. The semiconductor integrated circuit according to claim 4,  
further comprising:

a register that temporarily stores an address of the expected  
value storage when the result of the comparison indicates that the scan  
output data is inconsistent with the expected value.

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6. The semiconductor integrated circuit according to claim 5,  
wherein the comparison unit outputs the result of the comparison to the  
outside of the semiconductor integrated circuit, and the register outputs  
the address of the expected value storage to the outside of the

20 semiconductor integrated circuit.

7. The semiconductor integrated circuit according to claim 4,  
further comprising:

a register that temporarily stores an address of the scan output  
25 storage when the result of the comparison indicates that the scan

output data is inconsistent with the expected value.

8. The semiconductor integrated circuit according to claim 7,  
wherein the comparison unit outputs the result of the comparison to the  
5 outside of the semiconductor integrated circuit, and the register outputs  
the address of the scan output storage to the outside of the  
semiconductor integrated circuit.

9. The semiconductor integrated circuit according to claim 1,  
10 further comprising a phase locked loop that multiplies a clock signal  
input from the outside of the semiconductor integrated circuit and  
outputs the multiplied clock signal as a system clock to the scan target  
block of the semiconductor integrated circuit.

15 10. The semiconductor integrated circuit according to claim 1,  
wherein the scan target block receives scan input data from outside of  
the semiconductor integrated circuit, and  
the scan output storage outputs the parallel scan output data to  
outside of the semiconductor integrated circuit once the reception of the  
20 scan input data by the scan target block is over.